In the Claims:

1. A memory system comprising:

an array of addressable storage elements arranged in a plurality of rows and a plurality of columns; and

decoding circuitry coupled to the array of addressable storage elements, the decoding circuitry, responsive to decoding a first address, to access a first storage element of a first row of the plurality of rows, and the decoding circuitry, responsive to decoding a second address consecutive to the first address, to access a second storage element of a second row of the plurality of rows, the second row of the plurality of rows different from the first row of the plurality of rows.

2. A memory system according to claim 1 wherein each of the storage elements stores one bit.

3. A memory system according to claim 1 wherein each of the storage elements stores a plurality of bits arranged as a word.

4. A memory system according to claim 1 wherein each of the storage elements stores a plurality of bits arranged as a page.

5. A memory system according to claim 1 wherein the array of addressable storage elements comprises a plurality of nonvolatile memory cells.

6. A memory system comprising:

an array of storage elements arranged in a plurality of rows and a plurality of columns, each of the storage elements comprising an input and an output, each of the storage elements corresponding to a numeric address comprising more significant bits and less significant bits;

a column decoder coupled to the outputs of the storage elements of each of the plurality of columns, the column decoder operable responsive to at least one of the more significant bits; and

a row decoder coupled to the inputs of the storage elements of each of the plurality of rows, the row decoder operable responsive to at least one of the less significant bits.

7. A memory system according to claim 6 wherein

a) the input of each of the storage elements is a control gate, and

b) the output of each of the storage elements is a drain.

8. A memory system according to claim 6 wherein each of the storage elements stores one bit.

9. A memory system according to claim 6 wherein each of the storage elements stores a plurality of bits arranged as a word.

10. A memory system according to claim 6 wherein each of the storage elements stores a plurality of bits arranged as a page.

11. A memory system according to claim 6 wherein the array of storage elements comprises a plurality of nonvolatile memory cells.

12. A memory system according to claim 6 wherein each of the plurality of nonvolatile memory cells comprises a floating gate-type cell.

13. A memory system according to claim 6 wherein the at least one of the less significant bits comprises all of the less significant bits.

14. An embedded control system comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks, each of the plurality of blocks comprising:

an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and

decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second address consecutive to the first address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output.

15. An embedded control system according to claim 14 wherein the address signal comprises:

least significant bits representative of addresses of bits within a word,

next least significant bits representative of addresses of words within a page,

intermediate significant bits representative of addresses of the plurality of rows, the intermediate significant bits more significant than the next least significant bits,

more significant bits representative of addresses of pages within the plurality of rows, the more significant bits more significant than the intermediate significant bits, and

next more significant bits representative of addresses of the plurality of blocks, the next more significant bits more significant than the more significant bits.

16. A method of accessing a memory system, the memory system comprising an array of addressable storage elements arranged in a plurality of rows and a plurality of columns, the method comprising:

decoding a first address;

accessing, responsive to the first address, a first storage element of a first row of the plurality of rows;

decoding a second address, the second address consecutive to the first address; and

accessing, responsive to the second address, a second storage element of a second row of the plurality of rows, the second row of the plurality of rows different from the first row of the plurality of rows.

17. A method according to claim 16 wherein accessing a first storage element comprises reading a first page, the first page comprising a plurality of bits.

18. A method according to claim 17 wherein accessing a second storage element comprises reading a second page different from the first page, the second page comprising a plurality of bits.

19. A method according to claim 16 wherein accessing a first storage element comprises initiating a first burst access, the first burst access comprising a plurality of bits.

20. A method according to claim 19 wherein accessing a second storage element comprises initiating a second burst access different from the first burst access, the second burst access comprising a plurality of bits.

Sub B1 7

21. (New) The memory system of claim 6 wherein:
the numeric address comprises a group of bits;
the row decoder is operable responsive to a first portion of the group of bits;
the column decoder is operable responsive to a second portion of the group of bits, wherein each bit of the second portion is more significant than a least significant bit of the first portion.

A1

22. (New) The embedded control system of claim 14 wherein:
the address signal comprises a group of bits;
the row decoder is operable responsive to a first portion of the group of bits;
the column decoder is operable responsive to a second portion of the group of bits, wherein each bit of the second portion is more significant than a least significant bit of the first portion.